



SWIFT: Advancing Coexistence through a Cross-Layer Design Platform with an Adaptive Frequency-Selective Radio Front-End and Digital Algorithms

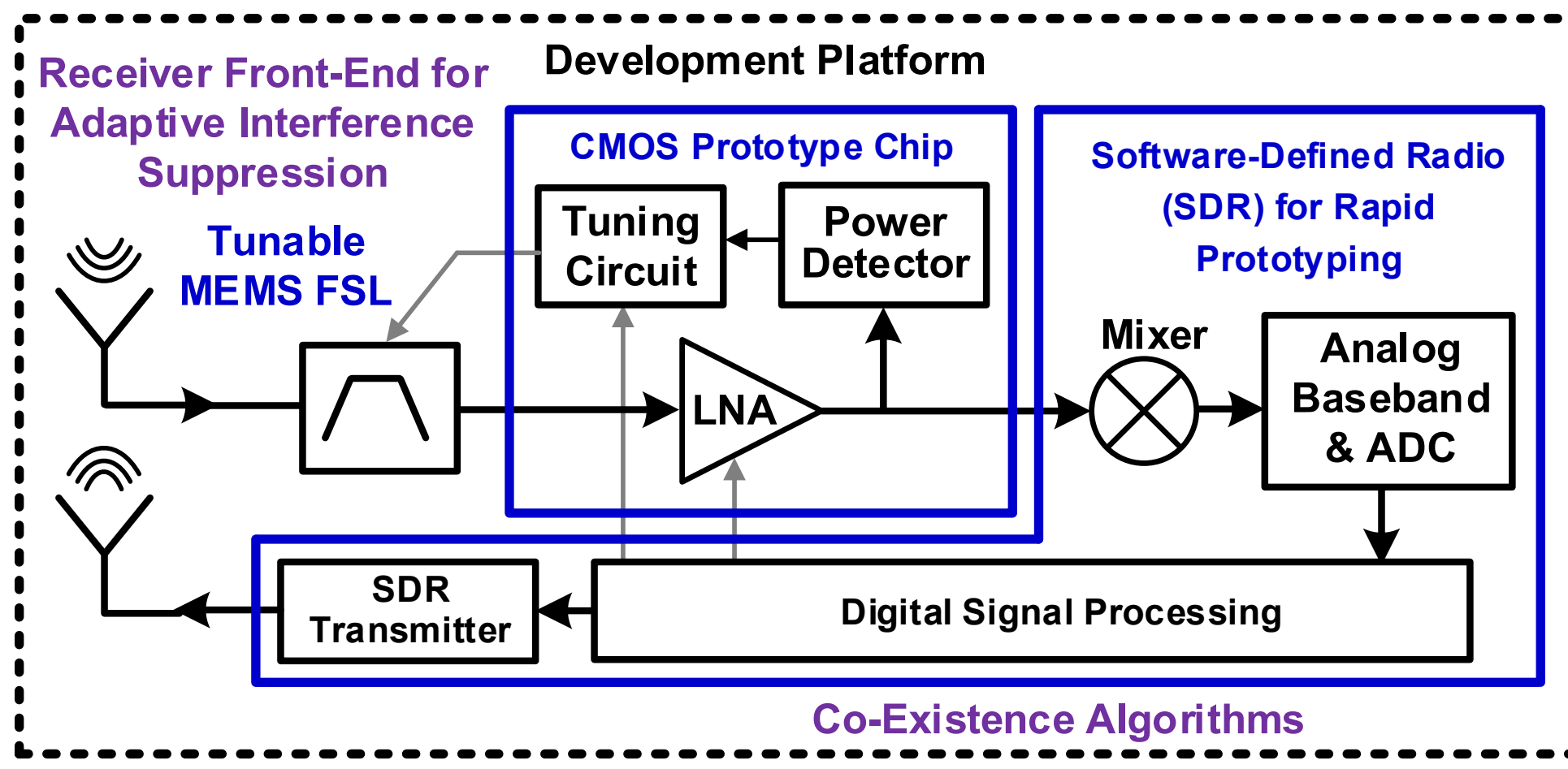
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Overview



Envisioned platform for the co-design of tunable MEMS frequency selective limiters (FSLs) for interference suppression, adaptable low-power CMOS front-end circuits, and digital algorithms.

This research aims to create a platform and first hardware prototypes for the co-design of next-generation RF receivers with the ability to suppress both in-channel and adjacent channel interferers without compromising the reception of desired signals. In crowded spectral environments, frequency selective limiters (FSLs) can intrinsically distinguish and attenuate interference characterized by power levels higher than a certain threshold. The research utilizes this fundamental capability through the development of fully integrated microelectromechanical system (MEMS) FSLs that can be manufactured with complementary metal-oxide-semiconductor (CMOS) process compatibility. Digital coexistence algorithms and adaptive analog front-end circuits will be conceived to strategically tune the operating points of the FSLs and of the receiver circuits towards the highest communication quality.

Project Summary

Goals

- Realization of FSLs with new monolithically integrated resonators having high quality factors ($Q > 2,000$). The acoustic properties of Aluminum Scandium Nitride (AlScN) thin-films and the ferroelectric properties of Hafnium Zirconium Oxide (HZO) atomic layers will be leveraged.
- Co-development of AlScN/HZO components with custom-designed analog circuits to achieve adaptive characteristics based on detected power levels, allowing to continuously optimize signal processing characteristics to changes in the surrounding electromagnetic spectrum.
- Design and fabrication of MEMS FSLs achieving 50 dB interference suppression combined with CMOS signal power detectors and tuning circuits consuming less than 50 μ W while converging in less than 10 μ s.
- Creation of algorithms to enhance coexistence with the ability to transmit waveforms in adjacent channels with very narrow guard bands. Incorporation of software-defined radios (SDRs) for fast prototyping and testing.

Approach

- Integrated FSL design using AlScN two-dimensional-mode resonators (2DMRs) to form two parametric frequency dividers (PFDs) and a wideband 90° Hybrid Coupler (HC), leveraging board-level PFD design methods.
- Analog circuits and digital processing will enable real-time reconfiguration of the FSL and of the low-noise amplifier's operating conditions based on monitoring under varying interference conditions. The tuning will optimize interference suppression within 1-30 MHz of the center frequency.
- General optimization for communication around 2.4 GHz with channel spacing in the 2-5 MHz range for proof-of-concept with Bluetooth Low Energy and Wi-Fi.

Intellectual Merit

- This research is establishing a framework for the co-design of RF front-ends with resilience to interference by leveraging the distinct features of CMOS circuits, AlScN/HZO components, digital algorithms and real-time calibrations.
- The outcomes will strengthen the resilience of wireless devices to both in-band and out-of-band interference, leading to adaptive radios for more efficient use of the available radio spectrum.
- Construction of a prototyping platform is underway to support the development of digital coexistence algorithms for cross-layer interference resilience.

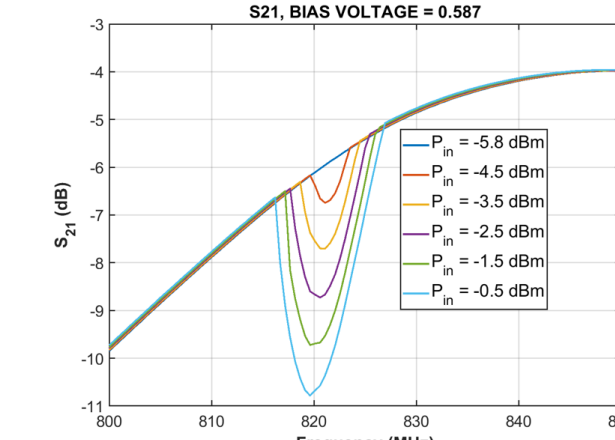
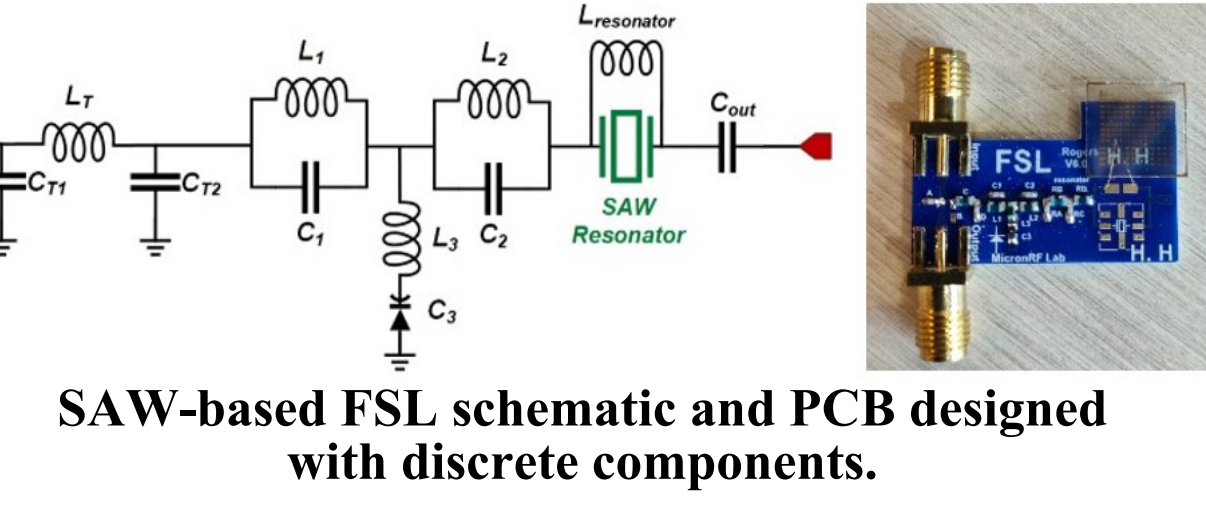
Broader Impacts

- The proposed research addresses the need to make low-power wireless receivers in IoT applications more immune to co-site interference and jamming.
- The design techniques will form the foundation for a new class of adaptive wireless systems with automatically tuned MEMS passives and analog circuits, which are digitally-controlled based on interference conditions.

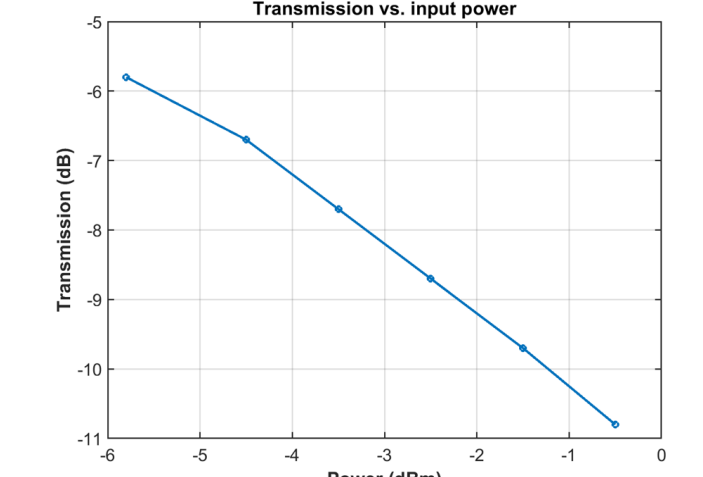
Recent Results

Demonstration of a SAW-based Frequency Selective Limiter (FSL) Prototype

- Proof-of-concept PCB
- Operation around 820 MHz
- SAW resonance frequency (f_R) of ~ 410 MHz
→ parametric notch at $2 \times f_R$ (i.e., ~ 820 MHz) for interference suppression



Measured transmission response (S_{21}) of the SAW-based FSL for multiple input power levels.

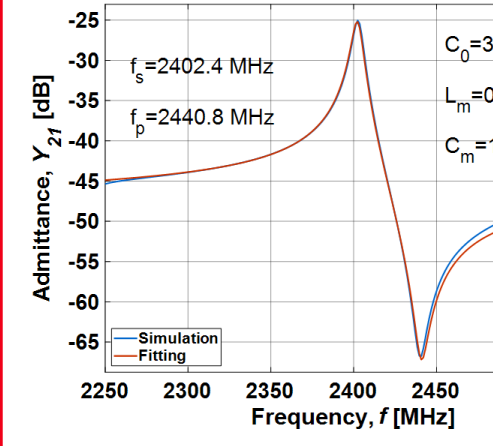


Measured transmission response (S_{21}) of the FSL at multiple input power levels.

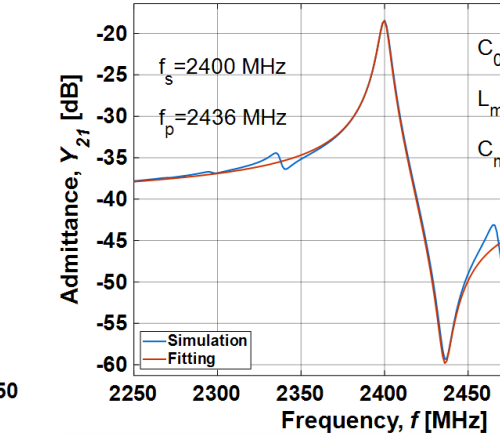
- 2.4GHz Contour Mode Resonator (CMR) design

→ C_0 tunability is achieved by changing the number of unit cells

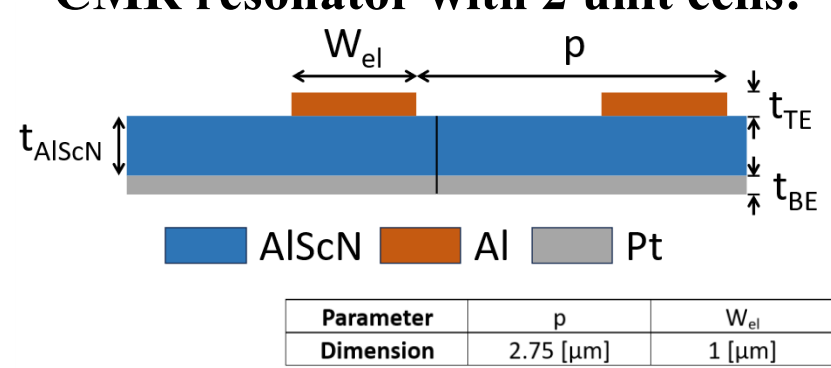
5 unit cells:



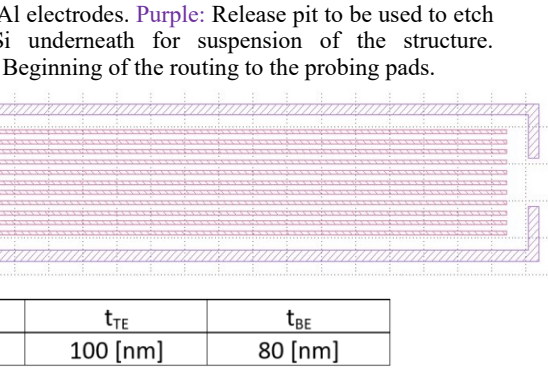
11 unit cells:



Cross-sectional view of a MEMS CMR resonator with 2 unit cells:

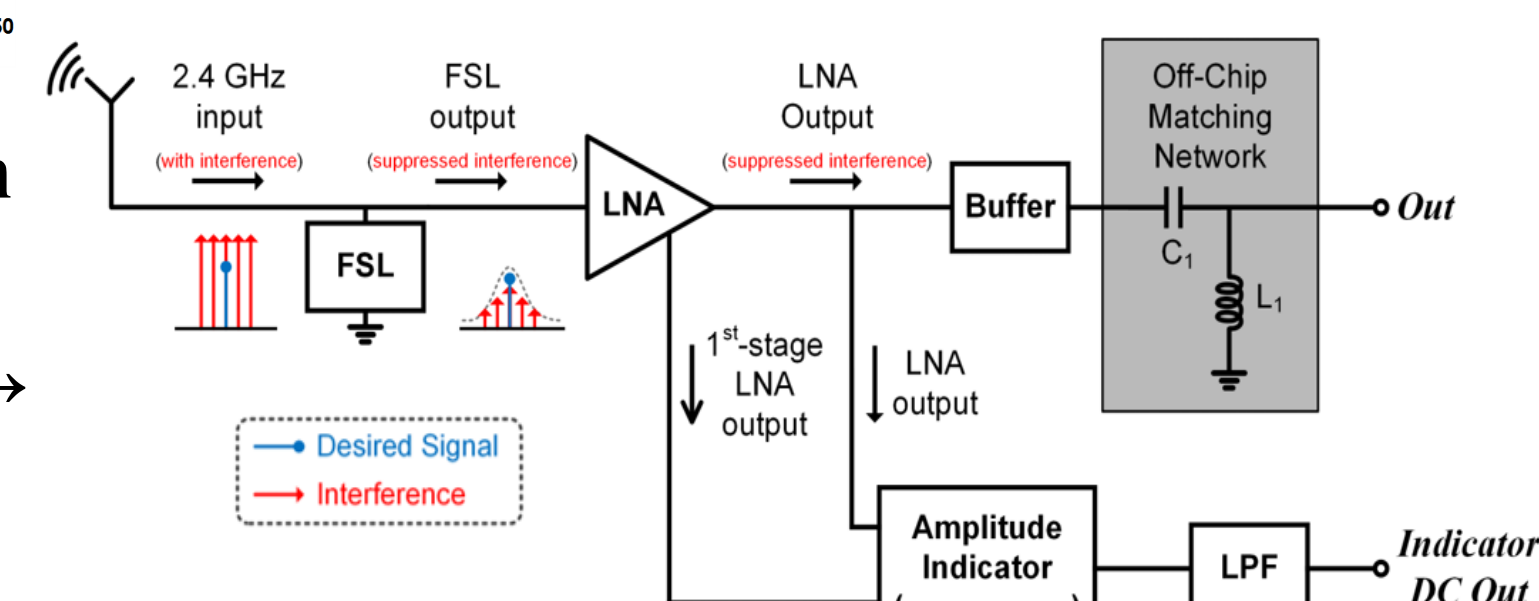


Layout of a resonator with 11 fingers:



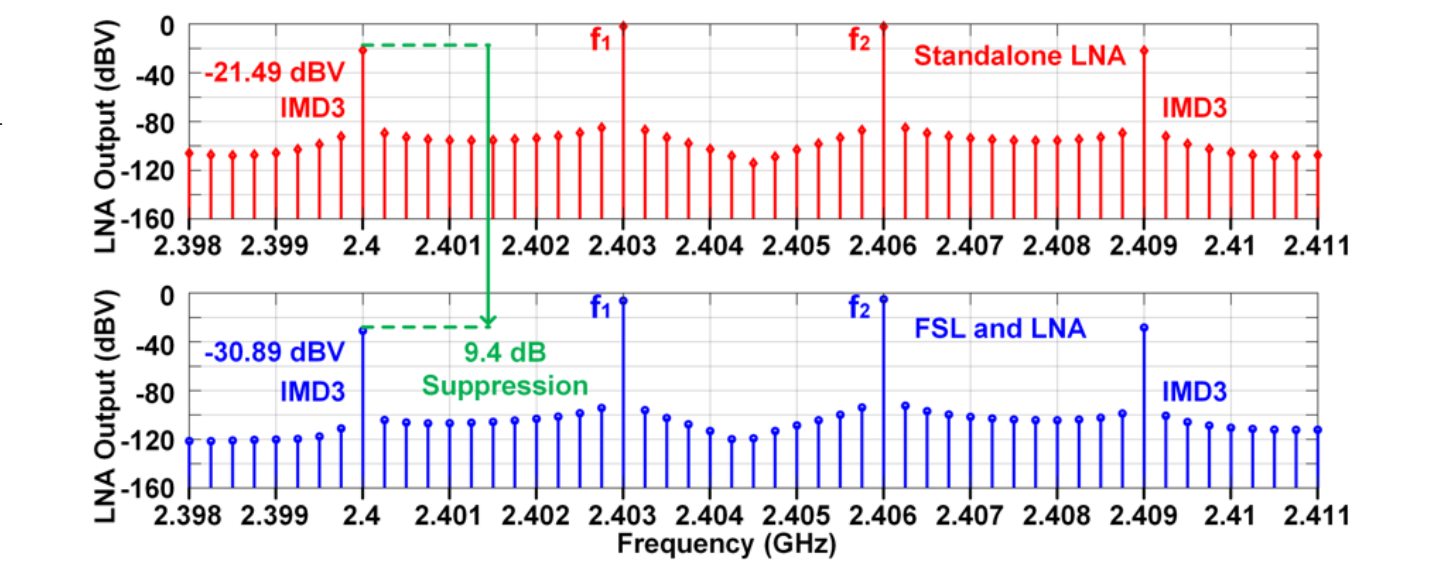
Low-Noise Amplifier (LNA) Design and Co-Simulation

- RF front-end under development → (with an FSL, CMOS LNA, and built-in amplitude indicator)



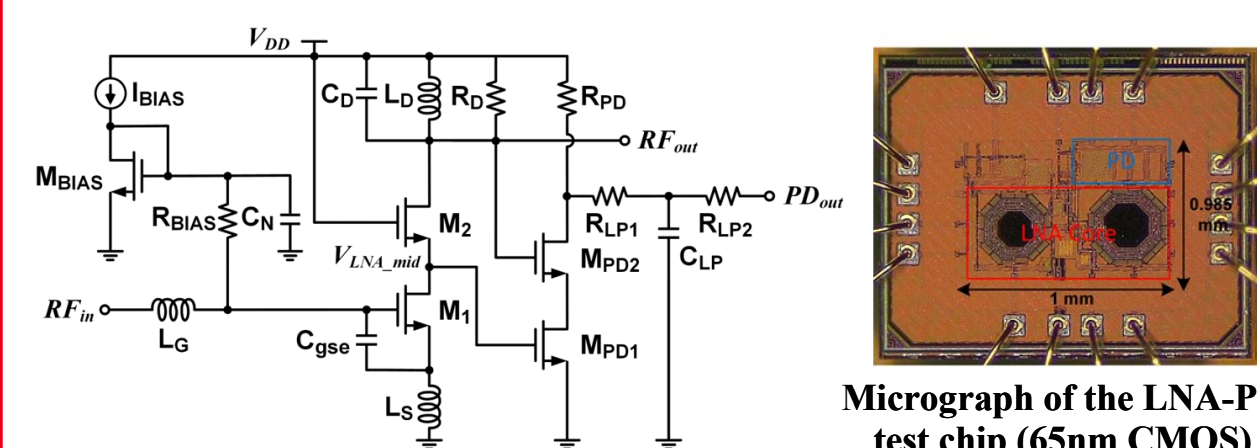
- The FSL can provide 9.4 dB reduction of the third-order intermodulation distortion (IMD3) components.

Simulation results →



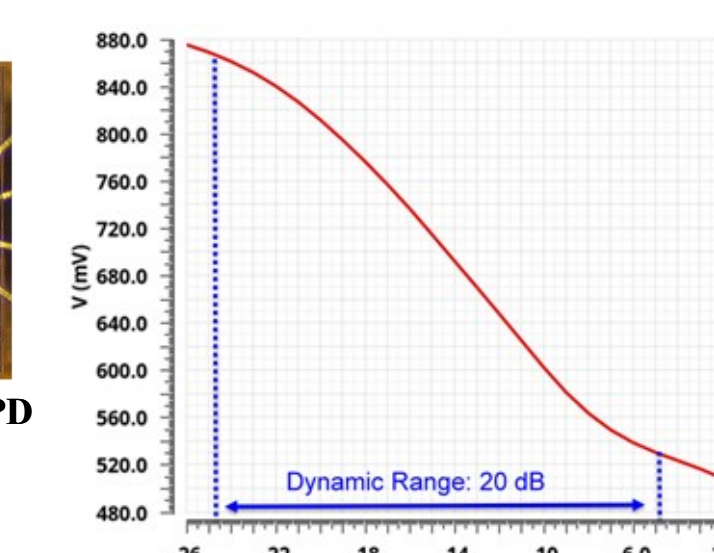
Simulated output spectrum of the standalone LNA (red) and the FSL/LNA combination (blue) from a test with two -10 dBm (-23 dBV) interference tones at 2.403 and 2.406 GHz.

- 2.4 GHz CMOS LNA designed with built-in power detection to monitor interference levels

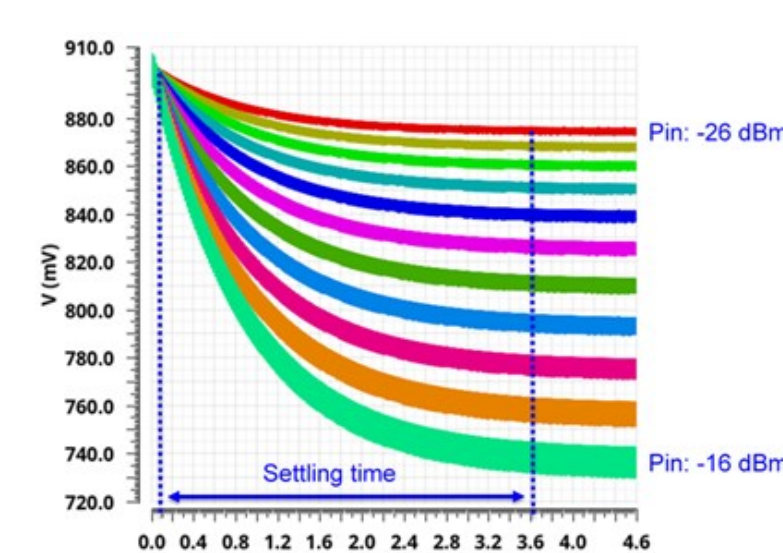


LNA (375 μ W) with built-in power detector (PD).

The PD leads to 0.4 dB S_{11} reduction and 25 μ W power increase, whereas other parameters were unchanged or slightly improved.



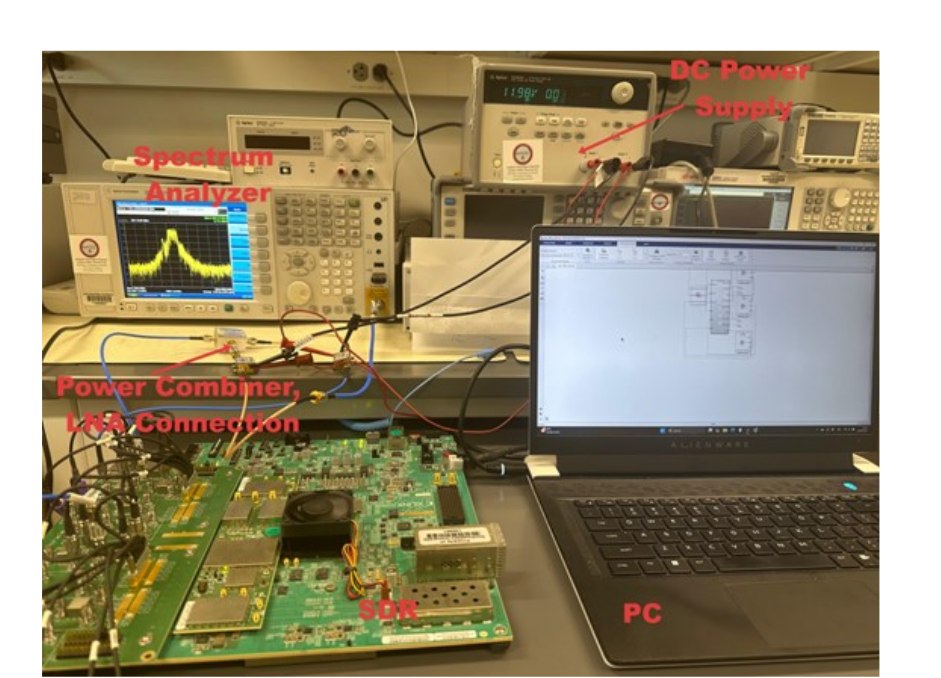
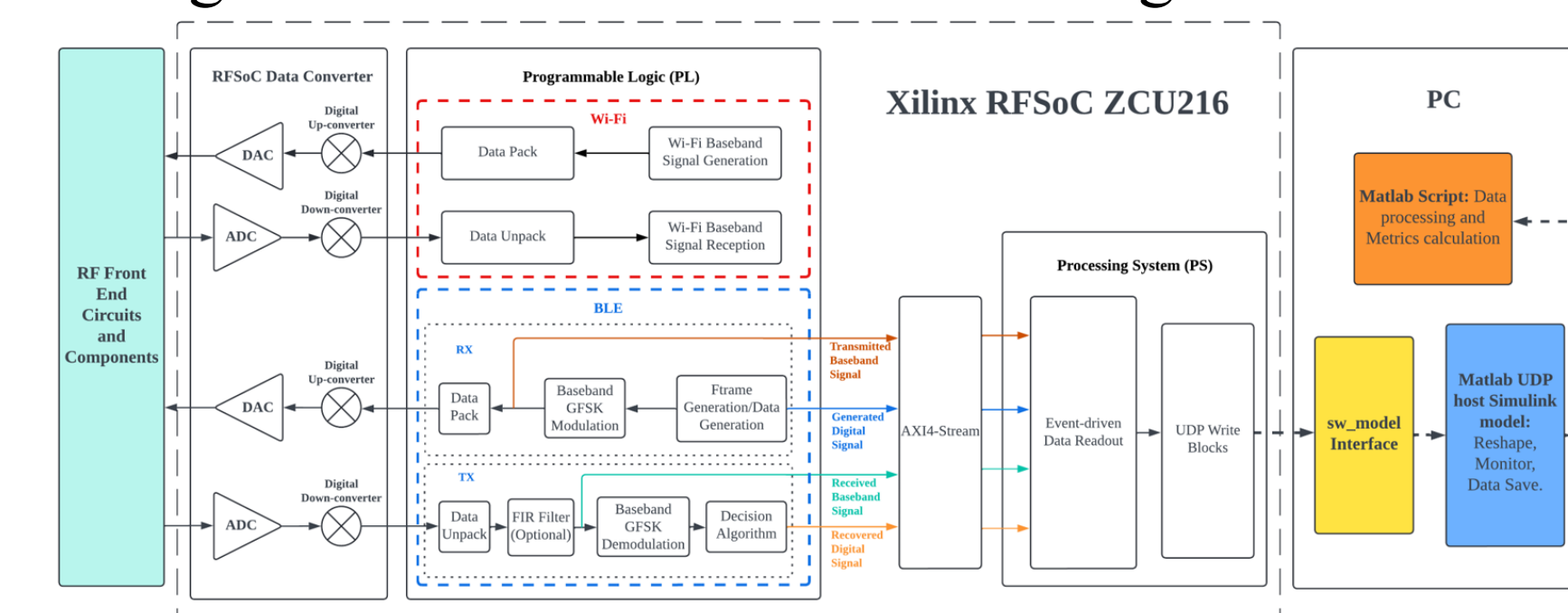
Simulated final PD output voltage vs. LNA input power.



Transient simulations of the PD, showing settling within 3.6 μ s.

Communication Algorithm Development for Xilinx RFSoc Implementations

- A prototyping platform was built based on a Xilinx RFSoc ZCU216 board and the MathWorks SoC Blockset workflow.
 - Incorporation of multiple BLE and Wi-Fi transmitter-receiver pairs
 - Demodulation and decoding of received signals with metrics such as BER & NMSE
 - Flexible adjustment of parameters (including center frequency, bandwidth, and power level of the generated BLE and Wi-Fi signals)
 - A digital FIR filter with configurable parameters is integrated into the BLE receiver as an optional feature
 - Matlab HDL Coder enables high-level design for FPGAs, SoCs, ASICs
 - Current experiments with an off-the-shelf LNA: assessment of BLE spectrum and demodulation with single-tone/two-tones sinusoidal interference signals, and with single and dual Wi-Fi interference signals



Future Work

- Fabrication completion and testing of 2.4 GHz MEMS resonators/FSLs
- Measurements of the 2.4 GHz CMOS LNA chip with built-in power detection
- Experimental demonstration of interference/IMD3 reduction with combined FSL and LNA prototypes
- Verification of BLE and Wi-Fi co-existence scenarios and improvements using FPGA-based algorithms and RFSoc hardware

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